Amendments to the Claims

This listing of claims will replace all prior versions of claims in this application:

1. (Original) A programmable logic device comprising:

digital signal processing circuitry comprising at least one embedded multiplier of a particular size; and

programmable logic circuitry, wherein a user logic design multiplier of a size greater than the particular size is implemented by a user logic design to hardware application using the at least one embedded multiplier and the programmable logic circuitry.

2. (Original) The programmable logic device of claim 1 wherein:

the programmable logic circuitry is configured to implement at least one component multiplier; and

the at least one component multiplier and the at least one embedded multiplier generate partial products, the sum of which is the product of the user logic design multiplier.

3. (Canceled)

4. (Original) The programmable logic device of claim 2 wherein the at least one component multiplier comprises three component multipliers implemented using programmable logic circuitry.

5. (Original) The programmable logic device of claim 2 wherein the at least one component multiplier comprises two component multipliers implemented using programmable logic circuitry.

6. (Original) The programmable logic device of claim 2 wherein:

the user logic design multiplier has a size that exceeds the particular size of the at least one embedded multiplier by one bit on one side of the at least one embedded multiplier; and

the at least one component multiplier comprises a single component multiplier implemented using programmable logic circuitry.

7. (Original) The programmable logic device of claim 2 further comprising circuitry for generating the sum of partial products of the at least one component multiplier and the at least one embedded multiplier.

8. (Currently Amended) The programmable logic device of claim 1 wherein the particular size is a largest size available among all embedded multipliers in the programmable logic device that is still smaller than the size of the user logic design multiplier.

9. - 17. (Canceled)

18. (Original) A printed circuit board on which is mounted a programmable logic device as defined in claim 1.

19. (Currently Amended) The printed circuit board defined in claim 18 further comprising:

a memory mounted on the printed circuit board and coupled to the ~~memory circuitry~~ programmable logic device.

20. (Currently Amended) The printed circuit board defined in claim 18 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the ~~memory circuitry~~ programmable logic device.

21. (New) The programmable logic device of claim 1, wherein the user logic design multiplier is used to implement an infinite impulse response filter.

22. (New) The programmable logic device of claim 1, wherein the user logic design multiplier is used to implement an finite impulse response filter.

23. (New) The programmable logic device of claim 2, further comprising bit shifting circuitry for shifting the output of one of the at least one component multiplier and the embedded multiplier.

24. (New) The programmable logic device of claim 2, further comprising bit padding circuitry for padding the output of one of the at least one component multiplier and the embedded multiplier.